IN THE CLAIMS:

A full listing of the claims, including any amendments made by this paper, is provided below:

28. (Currently Amended) A microstructure system including:

a wafer portion including a microstructure formed therein, located thereon or supported thereby wherein said wafer portion includes an upper wafer portion and a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, and wherein said microstructure is formed in or located on said upper wafer portion, and wherein said upper wafer portion defines a coverage area in top view; and

a solderable surface configured to receive an electronic component thereon in a direct attachment manner, said solderable surface being formed on, located on, or supported by said wafer portion, said solderable surface being electrically or operatively coupled to said microstructure such that an electronic component coupled to solderable surface can control, operate or receive inputs from at least part of said microstructure and wherein said solderable surface is formed or located on said lower wafer portion and is not located within said coverage area.

29. (Canceled)

30. (Canceled)

31. (Currently Amended) The microstructure system of claim ~~30~~ 28 wherein said upper wafer portion includes an outer perimeter, and wherein said outer perimeter defines said coverage area.

32. (Currently Amended) The microstructure system of claim ~~30~~ 28 wherein said lower

wafer portion has a coverage area in top view and wherein said coverage area of said upper wafer portion is entirely contained within said coverage area of said lower wafer portion.

33. (Amended) The microstructure system of claim 28 ~~wherein said wafer portion includes an upper wafer portion and a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, and wherein said microstructure is formed in or located on one of said upper or lower wafer portions, and wherein said solderable surface is formed or located on the other of said upper or lower wafer portion, and~~ wherein said upper and lower wafer portions are coupled together.

34. (Original) The microstructure system of claim 33 wherein said upper wafer and lower wafer portions are coupled together by a photopatternable adhesive.

35. (Original) The microstructure system of claim 34 wherein said photopatternable adhesive is benzocyclobutene.

36. (Currently Amended) The microstructure system of claim 33 wherein said upper wafer and lower wafer portions are coupled together by a relatively low reflow temperature adhesive, said adhesive having a reflow temperature of less than about 125° C.

37. (Original) The microstructure system of claim 28 wherein said solderable surface is a flip chip connection site configured to receive a chip thereon by flip chip bonding.

38. (Original) The microstructure system of claim 28 wherein said solderable surface includes a plurality of conductive pads, each pad being electrically isolated from any adjacent pad and having a melting point of less than about 250°C.

39. (Original) The microstructure system of claim 28 further including an electronic

component coupled to said solderable surface such that said electronic component can control, provide inputs to or receive outputs from said microstructure.

40. (Original) The microstructure system of claim 39 wherein said electronic component is a chip and wherein said chip is coupled to said solderable surface by flip chip bonding.

41. (Original) The microstructure system of claim 28 further including a plurality of solderable surfaces located on, or supported by said wafer portion, each solderable surface being electrically or operatively coupled to said microstructure.

42. (Original) The microstructure system of claim 41 further comprising a plurality of electronic components, each electronic component being coupled to one of said plurality of solderable surface, the system further including a controller coupled to said electronic components to control the input to or output from said electronic components via said solderable surfaces to thereby control or monitor the input to or output from said microstructure.

43. (Original) The microstructure system of claim 28 wherein said microstructure is at least one of a sensor or an actuator.

44. (Original) The microstructure system of claim 28 wherein said microstructure is a mirror array including a plurality of movable reflective surfaces.

45. (Original) The microstructure system of claim 44 further including at least one component which can control the movement of at least one of said reflective surfaces, wherein said solderable surface is electrically or operatively coupled to said at least one component.

46. (Currently Amended) The microstructure system of claim 45 wherein said component is an electrode for controlling the movement of said at least one movable reflective

surface when a voltage or current is applied across said electrode ~~and said at least one reflective surface~~.

47. (Currently Amended) The microstructure system of claim 46 wherein at least two electrodes are located below each of said reflective surfaces such that a voltage can be applied across said electrodes ~~and the associated reflective surfaces~~ to cause the associated reflective surface to move in at least two generally opposite directions.

48. (Original) The microstructure system of claim 44 wherein each reflective surface is individually movable relative to any adjacent reflective surfaces and is individually controllable.

49. (Original) The microstructure system claim 44 wherein said solderable surface can carry a sufficient bandwidth to allow a controller coupled to said solderable surface to cause and control the individual movement of each reflective surface relative to any adjacent reflective surfaces.

50. (Currently Amended) The microstructure system of ~~claim 44~~ claim 28 wherein ~~said wafer portion includes an upper wafer portion and a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, and wherein said mirror array is formed in or located on said upper wafer portion, and wherein said solderable surface is formed in, located on or supported by said lower wafer portion~~ said coverage area of said upper wafer portion is smaller than the coverage area of said lower wafer portion.

51. (Currently Amended) The microstructure system of claim ~~50~~ 44 wherein said upper wafer portion includes a silicon layer, and wherein said reflective surfaces are non-silicon material located on said silicon layer.

52. (Currently Amended) The microstructure system of claim ~~50~~ 44 wherein said upper

wafer portion includes a base portion and a plurality of movable portions rotatably coupled to base portion, and wherein each reflective surface is located on one of said movable portions.

53. (Currently Amended) The microstructure system of claim ~~50~~ 28 wherein said upper wafer portion includes at least a portion of at least one silicon-on-insulator wafer.

54. (Currently Amended) The microstructure system of claim ~~50~~ 28 wherein said lower wafer portion is or includes at least part of a semiconductor wafer, or a ceramic substrate, or a glass substrate, or a printed circuit board.

55 (Currently Amended) The microstructure system of claim ~~50~~ 28 wherein said lower wafer portion includes an upper surface facing said upper wafer portion, and wherein said solderable surface is located on said upper surface.

56. (Original) A microstructure system including:

an upper wafer or wafer portion including a microstructure formed therein, located thereon or supported thereby, said upper wafer portion defining a coverage area in top view; and

a lower wafer or wafer portion located generally below and coupled to said upper wafer or wafer portion, said lower wafer or wafer portion including an electronic component located thereon or supported thereby, said electronic component being electrically or operatively coupled to said microstructure such that said electronic component can control, operate or receive inputs from at least part of said microstructure, wherein said electronic component is generally not located within said coverage area of said upper wafer portion.

57-112. (Canceled)

113. (New) The microstructure system of claim 28 wherein said upper wafer portion and said lower wafer portion are coupled together by an electrically insulating material such that said upper and lower wafer portions are not directly electrically connected.

114. (New) The microstructure system of claim 39 wherein said electronic component is not located within said coverage area.

115. (New) The microstructure of claim 39 wherein said electronic component is positioned between said lower wafer portion and said upper wafer portion.

116. (New) The microstructure system of claim 28 wherein the entirety of said solderable surface is not located within said coverage area.

117. (New) The microstructure system of claim 56 wherein said lower wafer or wafer portion includes an upper surface facing said upper wafer or wafer portion, and wherein said solderable surface is located on said upper surface.

118. (New) A microstructure system including:

an upper wafer portion including a microstructure formed therein, located thereon or supported thereby, said upper wafer portion defining a coverage area in top view;

a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, said lower wafer portion including at least one electrode for controlling the movement of at least part of said microstructure;

a solderable surface formed or located on said lower wafer portion, wherein said solderable surface is not located within said coverage area; and

an electronic component coupled to said solderable surface by flip chip bonding and being electrically or operatively coupled to said electrode such that said electronic

component can control or operate said electrode to thereby control or operate said microstructure.

119. (New) The microstructure system of claim 118 wherein said upper wafer portion and said lower wafer portion are coupled together by an electrically insulating material such that said upper and lower wafer portions are not directly electrically connected.

120. (New) The microstructure system of claim 118 wherein said lower wafer portion includes an upper surface facing said upper wafer portion, and wherein said solderable surface is located on said upper surface.

121. (New) The microstructure of claim 118 wherein said electronic component is positioned between said lower wafer portion and said upper wafer portion.

122. (New) A microstructure system including:

an upper wafer portion including a microstructure formed therein, located thereon or supported thereby;

a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, said lower wafer portion including at least one electrode for controlling the movement of at least part of said microstructure;

a solderable surface formed or located on said lower wafer portion; and

an electronic component coupled to said solderable surface and being electrically or operatively coupled to said electrode such that said electronic component can control or operate said electrode to thereby control or operate said microstructure, wherein said electronic component is positioned generally between said upper and lower wafer portions.